AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A method of controlling a jitter buffer using a FIFO, comprising the steps of:

setting a packet delete area, a packet add area, and a clock control area inside the FIFO;

controlling a stored packet quantity of the FIFO to delete a specified packet when the stored packet quantity exceeds a lower limit of the packet delete area, and to always delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area;

controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to always add the packets when the stored packet quantity falls below a lower limit of the packet add area;

raising a clock frequency when the stored packet quantity of the FIFO reaches an upper limit of the clock control area;

lowering the clock frequency when the stored packet quantity of the FIFO reaches a lower limit of the clock control area; and

setting the clock control area between the packet add area and the packet delete area.

2. (Original) A method of controlling a jitter buffer as claimed in Claim 1, wherein the lower limit of the packet add area is coincident with the upper limit thereof.

3. (Original) A method of controlling a jitter buffer as claimed in Claim 1, wherein the lower limit of the packet delete area is coincident with the upper limit thereof.

4. (Original) A method of controlling a jitter buffer as claimed in Claim 1, wherein the lowering of the clock frequency is linear from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is linear from the lower limit of the clock control area to the upper limit thereof.

5. (Original) A method of controlling a jitter buffer as claimed in Claim 2, wherein the lowering of the clock frequency is linear from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is linear from the lower limit of the clock control area to the upper limit thereof.

6. (Original) A method of controlling a jitter buffer as claimed in Claim 3, wherein the lowering of the clock frequency is linear from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is linear from the lower limit of the clock control area to the upper limit thereof.

7. (Original) A method of controlling a jitter buffer as claimed in Claim 1, wherein the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is exponential from the lower limit of the clock control area to the upper limit thereof.

8. (Original) A method of controlling a jitter buffer as claimed in Claim 2, wherein the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is exponential from the lower limit of the clock control area to the upper limit thereof.

9. (Original) A method of controlling a jitter buffer as claimed in Claim 3, wherein the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is exponential from the lower limit of the clock control area to the upper limit thereof.

10. (Original) A device of controlling a jitter buffer, comprising:

a FIFO that configures the jitter buffer;

a packet deletion circuit provided on the input side of the FIFO;

a packet addition circuit provided on the output side of the FIFO;

a jitter buffer control circuit that includes a buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO, a VCO that supplies to vary a reproduced clock frequency, and a buffer control circuit for controlling the operations of the FIFO and peripheral circuits thereof, which controls the quantity of packets accumulated in the FIFO to delete the packets when the stored packet quantity exceeds a lower limit of a packet delete area, and controls to add the packets when the stored packet quantity falls below an upper limit of a packet add area; and

a decoder that accepts the packets outputted from the packet addition circuit, and decodes frames of the packets based on the clock frequency supplied from the VCO.

11. (Original) A device of controlling a jitter buffer as claimed in Claim 10, wherein a pulse width modulator is used in replacement for the VCO.

12. (Previously Presented) A device of controlling a jitter buffer as claimed in Claim 10, wherein the jitter buffer control circuit is in direct communication with the packet deletion circuit and the packet addition circuit

13. (Currently Amended) A device of controlling a jitter buffer as claimed in Claim 12, wherein the packet deletion circuit and the packet addition circuit are in direct communication ~~with the a buffer control circuit~~ with the buffer control circuit of the jitter buffer control circuit.

14. (Previously Presented) A device of controlling a jitter buffer as claimed in Claim 10, wherein the jitter buffer control circuit is in direct communication with the jitter buffer.

15. (Previously Presented) A device of controlling a jitter buffer as claimed in Claim 14, wherein the jitter buffer is in direct communication with a buffer monitoring portion of the jitter buffer control circuit.